Energy Minimization of Mobile Video Devices with a Hardware H.264/AVC Encoder Based on Energy-Rate-Distortion Optimization

Donghun Kang, Jungeon Lee, Jongpil Jung, Chul-Hee Lee and Chong-Min Kyung

ABSTRACT

In mobile video systems powered by battery, reducing the encoder’s compression energy consumption is critical to prolong its lifetime. Previous Energy-rate-distortion (E-R-D) optimization methods based on a software codec is not suitable for practical mobile camera systems because the energy consumption is too large and encoding rate is too low. In this paper, we propose an E-R-D model for the hardware codec based on the gate-level simulation framework to measure the switching activity and the energy consumption. From the proposed E-R-D model, an energy minimizing algorithm for mobile video camera sensor have been developed with the GOP (Group of Pictures) size and QP (Quantization Parameter) as run-time control variables. Our experimental results show that the proposed algorithm provides up to 31.76% of energy consumption saving while satisfying the rate and distortion constraints.

Keywords: energy minimization, video compression, energy-rate-distortion (E-R-D), H.264/AVC, power consumption, mobile video devices, hardware video encoder.

1. INTRODUCTION

Along with the emphasis on security, the demand for mobile surveillance cameras is growing. Battery-powered mobile video systems employ the video encoder to compress video input sequences. During the development of codec standards in last two decades, many groups studied rate and distortion optimization (RDO) in pursuit of compression efficiency. However, such effort is not enough in the case of mobile camera systems because energy constraint has become a dominant issue over rate and distortion constraints. In order to improve mobile cameras’ lifetime, system designers need to consider both a low-power hardware design and a low-power operation method such as the E–R–D optimization.

Recent progress on low-power and low-cost semiconductor technology has allowed for low-power operating mobile camera systems. However, E-R-D optimization method has the edge over such technology because it saves more energy. E–R–D optimization involves three variables i.e., energy, rate and distortion. Figure 1 is the block diagram of E–R–D optimization for a H.264/AVC encoder. The E–R–D optimizer made of microprocessors is monitoring the encoder’s power, rate and distortion. To optimize the encoder’s performance, the E–R–D optimizer calculates the optimum encoder parameters, i.e., QP, GOP size, rate control algorithm(Constant bit-rate or variable bit-rate), motion estimation methods, entropy coding methods(CAVLC or CABAC) and so on, and accordingly controls the encoder. E–R–D optimizing process is done by run-time.

Because battery-based mobile video systems have constraints on power consumption, it is necessary to use a hardware codec to achieve a performance up to 30fps in our target system. However, most previous E–R–D optimizers for mobile video communication devices were proposed with software codecs which are executed by microprocessors (Intel Pentium III and Intel XScale processor) [1], [2]. Therefore it was not suitable for common use in terms of performance – 5 fps [2]. For microprocessors, the measurement of an encoder’s power consumption is based on computational workload. This kind of power model based on a software codec with complexity mapping may have different characteristics from that based on a hardware codec which is used in real world systems. Moreover, a hardware codec has very restricted power scalability in general because of its increased logic size. Therefore, it is necessary to select power scalable parameters and suggest an E-R-D model based on hardware encoder codec.

In [3], Kim et al. tried to verify the power model for the hardware H.264/AVC codec. Register-transfer level (RTL) power estimation is done based on its gate size with technology information. In their works, RTL is implemented with an

1 dhkang@vslab.kaist.ac.kr
encoder’s functional blocks and estimated with its gate size. Estimated powers of each functional blocks are executed along with JM software H.264/AVC codec and DRAM model. However, the power model has to be analyzed with a fully implemented hardware codec along with switching activity like a low-power mobile video device.

In this paper, the E–R–D model of the hardware implemented H.264/AVC encoder is proposed to minimize the energy consumption of the mobile video system. Our work is comprised of two folds. First, we estimate the E–R–D model with the hardware codec which can be practically used in low-power mobile video systems. Second, we propose the energy minimization algorithm based on E–R–D optimization which can apply to real implementation.

The rest of the paper is as follows. Section 2 describes the target system. The framework of the E–R–D modeling and the estimated E–R–D model are described in Section 3. The energy minimization algorithm is proposed in Section 4, and its experimental results are presented in Section 5, followed by the conclusion in Section 6.

2. TARGET SYSTEM

Our target system is a battery based mobile video devices. Figure 2 shows the main functional blocks of our systems. In this system, input video sequences are captured by a CMOS image sensor (CIS) module. The video sequences are compressed by the H.264/AVC encoder. During video encoding, the encoder sends rate and distortion information as monitoring values and receives optimized GOP size and QP from the host processor called the ‘E–R–D controller’. This controller also simultaneously considers energy, rate and distortion constraints which are monitored by a battery, Wi-Fi and Storage modules. Compressed video sequences are stored or transmitted by storage or Wi-Fi module. To implement our target system containing above functional blocks, we have to consider key characteristics for the system. First, because the target system captures video by CIS module in mobile environment, the encoder and other functional blocks have to be adapted to various sequences with E–R–D optimization. Since our system is operated by the battery, secondly, we have to apply the low-power operation policy to maximize the lifetime. Finally, the target camera systems are used as a mobile video device application. Therefore, we have to consider rate and distortion constraints to guarantee awareness.

3. ENERGY-RATE-DISTORTION MODELING

3.1 Modeling Framework

For E–R–D modeling, we created a test bench comprised of a CPU, an encoder and a bus. The CPU is operated as the E–R–D controller. Along with the E–R–D optimization, the encoder compresses sequences and makes switching activity information of each functional block. To facilitate the encoder’s operation, we utilize the fully implemented hardware.
H.264/AVC encoder. Figure 3 is the diagram of functional blocks of the H.264/AVC encoder. The bus transfers data, i.e., input sequences, reconstruction images, monitoring values and streams, to all modules. Figure 2 (b) shows the energy modeling with gate-level simulation. After synthesis of the RTL source code, power analysis is done with synthesized netlist, constraints and switching activity. The power modeling process requires not only the encoder’s but also its SRAM buffer’s power consumption.

To implement specific encoding behaviors, we control encoding parameters according to input sequences. However, the hardware encoder has very restricted power scalable parameters. We select GOP size as a power scalable parameter because intra and inter frames have different power consumptions. QP also can be a power scalable parameter since it affects rate and distortion. In this work, we select GOP size and QP as power scalable parameters to control energy, rate and distortion. Power, rate and distortion are monitored with GOP size and QP at every frame.

Figure 2. (a) The block diagram of the fully implemented hardware H.264/AVC encoder. The encoder have 850k gates under synthesis condition of worst case and 40% timing overhead for wire load delay with Samsung 65nm LP technology library. (b) The process of the energy modeling of the encoder through the gate-level simulation.

### 3.2 Effects on Power-Rate by GOP size

GOP size is the parameter determined by the distance between two neighbor intra-frames (I-frames) which means encoded only with intra prediction. Our H.264/AVC encoder implements clock gating techniques for inter prediction’s motion estimation (ME) and motion compensation (MC) modules. Because ME and MC for inter prediction takes about 50~70% of complexity in encoder, therefore, GOP size can be a powerful energy scalable parameter.

Figure 4 shows the average power consumption (mW), number of bits of the encoder for I-frames and P-frames, respectively. From the above power-GOP size and rate–GOP size relationships, we can formulate the P–R model. Bit-rate $R_{enc}$ is expressed as follows.

$$R_{enc} = \bar{b}_i \times n_i + \bar{b}_p \times (f - n_i)$$ (1)

where $\bar{b}_i$ and $\bar{b}_p$ are the number of bits for I-frame and P-frame, respectively. $f$ is the number of frames per second. The number of intra frames are expressed as follows.

$$n_i = \begin{cases} \frac{f}{s_g} & \text{if } \text{mod}(r_f, s_g) = 0 \\ \left\lfloor \frac{f}{s_g} \right\rfloor + 1 & \text{if } \text{mod}(r_f, s_g) \neq 0 \end{cases}$$ (2)
where $s_g$ is GOP size.

$P_{enc}$ stands for the encoder’s power consumption. It can be expressed as follows.

$$ P_{enc} = \bar{P}_I \times \frac{n_I}{T} + \bar{P}_P \times \left(1 - \frac{n_I}{T}\right) $$

From combining (1) and (3) in terms of GOP size, we can notice that P-R model is given by

$$ P_{enc} = c_{enc}^1 \times R + c_{enc}^2 $$

where

$$ c_{enc}^1 = \frac{\bar{P}_I - \bar{P}_P}{f(b_1 - b_P)} $$

$$ c_{enc}^2 = \bar{P}_P - \frac{\bar{P}_P(b_1 - b_P)}{b_1 - b_P} $$

In a video sequence, 1 second is small enough to assume that almost frames have similar power, rate and distortion characteristics, i.e., $b \approx \bar{b}$ and $P \approx \bar{P}$.

![Figure 3](http://proceedings.spiedigitallibrary.org/)

**Figure 3.** The average power consumption and the number of bits for the first 30 frames of foreman, akiyo, bus and mobile sequence when GOP size is 30 and QP is 26; (a) power consumption, (b) the number of bits.

### 3.3 Effects on Power-Distortion by QP

In [11], K. Takagi et al. show that QP-distortion has linear models and QP-rate has exponential models. Therefore, we can express distortion $D$ in PSNR (dB) with QP as follows.

$$ D_{PSNR} = c_{qp}^1 \times QP + c_{qp}^2 $$

where $c_{qp}^1$ and $c_{qp}^2$ are fitting parameters for QP – D model.

Figure 4 denotes the power consumption while QP is varies from 26 to 32. The variation of a power consumption is below 1% of the power consumption of the encoder. It means that QP cannot be used as the power scalable parameter in the hardware encoder.
3.4 E-R-D Modeling with GOP size and QP

We already notice that the power scalable parameter is not QP but GOP. We are here concerned with GOP size and QP in the P-D model. Figure 5 shows the P–D model for I frames and P-frames of foreman, akiyo, mobile and bus when QP is 26. Each point is the average power and distortion of GOP when GOP size is 5. We can notice that the relationship between power and distortion which is represented with mean square error (MSE) is polynomial. Therefore, we can formulate P–D model for I-frames and P-frames as follows.

\[
P_i = c_{mse,i}^1 \times (D_{mse,i})^2 + c_{mse,i}^2 \times D_{mse,i} + c_{mse,i}^3
\]

\[
P_p = c_{mse,p}^1 \times (D_{mse,p})^2 + c_{mse,p}^2 \times D_{mse,p} + c_{mse,p}^3
\]

\(P_i, D_{mse,i}, P_p, D_{mse,p}\) are power consumption and distortion (MSE) for I-frames and P-frames, respectively. \(c_{mse,i}^1, c_{mse,i}^2, c_{mse,i}^3, c_{mse,p}^1, c_{mse,p}^2, c_{mse,p}^3\) are fitting parameters. We can work out the P-R-D model from Equation (4), (7), (8) and (9). After all, the estimated P-R-D model can be considered as E-R-D model in terms of encoding time.
3.5 E-R-D Modeling with DRAM

The energy consumption of the encoder is related to not only the operation of the encoder with SRAM but also with the external DRAM. Table 1 shows that number of accesses for the external DRAM with a full HD sequence in 30 fps and a 10Mbps stream. The H.264/AVC encoder has four accesses for the external DRAM, i.e., current image read, reference image read, reconstruction image write and stream write. We realize that the number of accesses for the stream write which is related to QP takes up only 0.4% of the total number of accesses. Because LPDDR2 4GB DRAM only takes about 30mW to compress a full HD video, 0.12mW is only a marginal number compared to the total power consumption of the encoder. However, GOP size is the power scalable parameter on DRAM because I-frame does not require access to the reference frame memory; in fact, 42.7% of DRAM accesses do not belong to the P-frame. Therefore, the P–D model with the DRAM can be formulated by GOP size just as the encoder’s P–D model.

From what has been stated above, we can write $P_{tot}$, which stands for the power consumption of the encoder, as follows.

$$P_{dram} = P_{dram,i} \times \frac{n_i}{f} + P_{dram,p} \times \left(1 - \frac{n_i}{f}\right)$$  \hspace{1cm} (10)

$$P_{tot} = P_{enc} + P_{dram}$$

$$= c_1^{tot} \times R + c_2^{tot}$$  \hspace{1cm} (11)

where $P_{dram}$ is the power consumption of DRAM.

$$c_1^{tot} = \frac{P_{dram,i} + P_p - (P_{dram,p} + P_p)}{r_{i-p}}$$  \hspace{1cm} (12)

$$c_2^{tot} = \frac{P_{dram,i} + P_p - (P_{dram,p} + P_p)}{r_{i-p}} \times r_p + P_p$$  \hspace{1cm} (13)

$P_{dram,i}$ and $P_{dram,p}$ are DRAM power consumptions for I-frames and P-frames, respectively, and $c_1^{tot}$ and $c_2^{tot}$ are fitting parameters for power consumption for the encoder with DRAM.

Table 1. Number of DRAM accesses when the encoder compress a 10 Mbps full HD (1920x1080) sequence with 30 fps.

<table>
<thead>
<tr>
<th>BUS</th>
<th>AXI 64</th>
</tr>
</thead>
<tbody>
<tr>
<td>Request Information</td>
<td>Number of Request/Sec</td>
</tr>
<tr>
<td><strong>Current Frame Read</strong></td>
<td>Y</td>
</tr>
<tr>
<td></td>
<td>C</td>
</tr>
<tr>
<td><strong>Reference Frame Read</strong></td>
<td>Y</td>
</tr>
<tr>
<td></td>
<td>C</td>
</tr>
<tr>
<td><strong>Reconstruction Frame Write</strong></td>
<td>Y</td>
</tr>
<tr>
<td></td>
<td>C</td>
</tr>
<tr>
<td><strong>Stream Write</strong></td>
<td></td>
</tr>
<tr>
<td><strong>Total requests</strong></td>
<td></td>
</tr>
</tbody>
</table>
4. PROPOSED METHOD

4.1 System Model

In existing energy minimization algorithms, the assumptions on distortion were made in order to simplify the optimization problem [2]. They assumed that the video sequence is encoded with a constant target distortion. However, this assumption is not entirely correct due to the encoder’s scene-dependency, which we described in section 3. Distortion changes along with encoding scenes and it is difficult to maintain the constant distortion. We have to introduce a method to control the distortion with a constant target distortion regardless of scene changes. Moreover, we found out that the hardware codec’s power scalability is different from that of the software codec. Therefore, we have to define system energy model with the encoder, transmission and storage.

To implement constant distortion, as shown in Figure 1, we add ‘MSE calculation module’ to monitor distortion. We design the MSE calculation module before the de-blocking filter to reduce the number DRAM accesses. Because the influence of the de-blocking filter in distortion is only marginal [10], proposed method can be used in video encoding. After adding the MSE calculation module, the encoder increases only 0.3% in gate size and 0.4~0.9% in power consumption, which are still insignificant figures.

![Figure 6. The Power-Rate measurement and model for the Samsung 32GB SD card class 6.](image)

![Figure 7. Power-Rate relationship of the target system when |ε₁| is smaller than |ε₂|.](image)

We already found the linear P–R model with the power scalable parameter GOP size including DRAM power consumption in Equation (11). From the measurement of power consumption in Figure 6, we can derive the linear P-R model of the storage. With the linear P-R models of storage and transmission [9], we can formulate the P–R model of the target system as follows.

For the system using the transmission and/or the storage module,
\[ P_{sys} = (c_{ts}^1 + c_{total}^1) \times R_{enc} + c_{total}^2 + c_{ts}^2 \]  

(14)

where the power consumption of the transmission or the storage module, \( P_{ts} \) is

\[ P_{ts} = c_{ts}^1 \times R_{enc} + c_{ts}^2 \]  

(15)

\( c_{ts}^1 \) and \( c_{ts}^2 \) are fitting parameters for the transmission or the storage module.

Figure 7 shows the P-R model of our target system. Because the P-D model is linear, \( R_{opt} \) representing the optimized bit-rate is determined by \( c_{tot}^1 \) and \( c_{ts} \). \( R_{opt} \) would be the maximum bit-rate of the encoder meaning the GOP size would be 1. However, \( R_{opt} \) is limited by the channel condition and storage’s maximum read/write speed and capacity. The battery can also create a constraint on distortion. In the case of low battery, as shown in Section 3.4, the target distortion can be limited.

### 4.2 Algorithm Implementation

From E-R-D model for the hardware encoder, we propose the algorithm to minimize energy using GOP size and QP controlling with constraints on rate and distortion. Adaptive GOP size controlling algorithm was introduced to improve rate and distortion characteristics [5], [6]. However, these efforts were not for energy minimizing and it didn’t concern both rate control and constant distortion. To maintain a constant distortion, the sequence based constant quality control using mean absolute difference and PSNR is done by on-the-fly [7], [8]. This kind of method is necessary for our system because our target system has a target distortion. We also need to consider constant bit-rate control because maximum bit-rate \( R_{opt} \) is necessary. However, the conventional CBR algorithm cannot control distortion according to variation of scenes. Therefore, we can formulate our algorithm as follows.

\[ (s_{g, opt}, q_{opt}) = \underset{(s_g, q)}{\arg \min} P_{sys} (R_{enc}, D) \]  

(16)

such that \( R < R_{opt}, D \approx D_t \)

\( s_{g, opt} \) and \( q_{opt} \) are the optimized GOP size and QP to minimize energy. \( D_t \) is the target distortion.

Figure 8 shows the flowchart of the proposed algorithm. \( i \) is the GOP number. From the beginning, the algorithm checks whether it is the first GOP. If it is true, the encoder compresses a sequence with initial QP and GOP size. After encoding the first GOP, QP of second GOP is updated. \( q_2 \) which is the QP of second GOP is determined by followed condition.

\[ q_2 = \begin{cases} q_{init} + 1 & (D_1 < D_t) \\ q_{init} - 1 & (D_1 > D_t) \end{cases} \]  

(17)

where \( q_{init} \) is the initial QP and \( D_1 \) is the distortion of the first GOP. From the second GOP, algorithm calculate the GOP size along with the encoding process of P-frames. \( s_{g, opt} \) which means the optimal GOP size, is determined as follows.

\[ b_{surplus} = b_1 - b_{assigned}, \text{then } j = s_{g, opt} \]  

(18)

\[ 2 \text{ We assume that our target system is satisfied with this condition. In general, this condition is quite valid for mobile video devices. As shown in Figure 6, for example, Samsung 32GB SD card consumes 53.6~64.6 mW with 64.7~996.0 kB/s. In this condition, } |c_{ts}| \text{ is definitely smaller than } |c_{tot}^1| \text{ of our target system.} \]
\[ b_{\text{surplus}} = \sum_{j=2}^{l}(b_{\text{assigned}} - b_j) \]  
\[ b_{\text{assigned}} = \frac{b_{\text{opt}}}{I} \]  

\( b_1 \) is the number of bits of the first I-frame of \( i \)th GOP. \( b_{\text{opt}} \) is the number of bits for the second one when bit-rate is \( R_{\text{opt}} \). \( b_{\text{assigned}} \) and \( b_{\text{surplus}} \) represent the number of assigned and surplus bits for P-frames, respectively. After GOP controlling, QP-Distortion modeling is done for QP updating as follows.

\[
q_i = \begin{cases} 
q_{i-1} + 2 & (D_{i-1} < 0, \ (D_i - D_{i-1}) < 2c_q^1) \\
q_{i-1} + 1 & (D_{i-1} < 0, c_q^1 < (D_i - D_{i-1}) < 2c_q^1) \\
q_{i-1} & (D_i - D_{i-1}) < 1 \left| c_q^1 \right| \\
q_{i-1} - 1 & (D_{i-1} > 0, c_q^1 < (D_i - D_{i-1}) < 2c_q^1) \\
q_{i-1} - 2 & (D_{i-1} < 0, (D_i - D_{i-1}) > 2c_q^1) 
\end{cases}
\]  

(21)

where \( q_i \) and \( D_i \) is the QP and PSNR of the \( i \)th GOP, respectively.

\[ c_q^1 = \frac{D_{i-1} - D_{\text{past}}}{q_{i-1} - q_{\text{past}}} \]  
\[ c_q^2 = D_{i-1} - \frac{q_{\text{past}}(D_{i-1} - D_{\text{past}})}{q_{i-1} - q_{\text{past}}} \]  

(22)  
(23)

which are calculated by Equation (7). \( c_q^1, c_q^2 \) are fitting parameters of the QP-D model, \( q_m \) and \( D_m \) are QP and PSNR of the QP-D model. \( q_{\text{past}} \) is the past QP which is not same as \( q_{i-1} \). And \( D_{\text{past}} \) is the PSNR of the GOP, which has \( q_{\text{past}} \).

---

![Flowchart of the proposed energy minimization algorithm](image-url)
5. EXPERIMENTAL RESULTS

For the foreman sequence with cif resolution, as shown in Figure 9, the proposed algorithm saves 10.26% more energy compared to CBR when the target bit-rate and distortion are 500Kb and 33 dB, respectively. This result signifies that the proposed algorithm creates a distortion that is consistent with the target distortion compared to non-distortion scalability of CBR.

Figure 9 Distortion (PSNR) comparison between CBR and proposed algorithm in terms of sequences, target distortion and bit-rate; foreman.cif, 33 dB, 500 Kb

Figure 10 shows energy consumption saving of the first 90 frames of foreman, akiyo, mobile, bus, coastguard and stefan sequences compared with the conventional CBR encoding algorithm which is generally used in video codec. According to various bit-rate, proposed method has various energy consumption saving results when the target PSNR distortion is 31dB. Proposed method shows 1.7 to 31.76 % of energy consumption saving.

Table 2. The number of I-frames and energy consumption percentage for the first 90 frames of foreman, akiyo, bus, mobile, stefan and coastguard sequences according to various rate when the target PSNR distortion is 31dB.

<table>
<thead>
<tr>
<th>Sequence</th>
<th>Bit-rate (kB)</th>
<th># of I-frames</th>
<th>Energy Saving (%)</th>
<th>Sequence</th>
<th>Bit-rate (kB)</th>
<th># of I-frames</th>
<th>Energy Saving (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>foreman</td>
<td>350</td>
<td>13</td>
<td>5.82</td>
<td>stefan</td>
<td>900</td>
<td>9</td>
<td>5.02</td>
</tr>
<tr>
<td></td>
<td>400</td>
<td>17</td>
<td>10.94</td>
<td></td>
<td>1000</td>
<td>11</td>
<td>6.2</td>
</tr>
<tr>
<td></td>
<td>450</td>
<td>25</td>
<td>16.89</td>
<td></td>
<td>1100</td>
<td>13</td>
<td>8.05</td>
</tr>
<tr>
<td></td>
<td>500</td>
<td>34</td>
<td>24.6</td>
<td></td>
<td>1200</td>
<td>16</td>
<td>12.3</td>
</tr>
<tr>
<td>akiyo</td>
<td>150</td>
<td>14</td>
<td>8.19</td>
<td>coastguard</td>
<td>900</td>
<td>10</td>
<td>3.42</td>
</tr>
<tr>
<td></td>
<td>200</td>
<td>23</td>
<td>16.19</td>
<td></td>
<td>1000</td>
<td>14</td>
<td>9.54</td>
</tr>
<tr>
<td></td>
<td>250</td>
<td>27</td>
<td>20.01</td>
<td></td>
<td>1100</td>
<td>24</td>
<td>20.67</td>
</tr>
<tr>
<td></td>
<td>300</td>
<td>41</td>
<td>31.76</td>
<td></td>
<td>1200</td>
<td>30</td>
<td>26.36</td>
</tr>
<tr>
<td>bus</td>
<td>1000</td>
<td>7</td>
<td>3.28</td>
<td>mobile</td>
<td>1600</td>
<td>5</td>
<td>1.7</td>
</tr>
<tr>
<td></td>
<td>1100</td>
<td>10</td>
<td>5.69</td>
<td></td>
<td>1800</td>
<td>7</td>
<td>3.31</td>
</tr>
<tr>
<td></td>
<td>1200</td>
<td>18</td>
<td>15.97</td>
<td></td>
<td>2000</td>
<td>13</td>
<td>12.03</td>
</tr>
<tr>
<td></td>
<td>1300</td>
<td>19</td>
<td>16.29</td>
<td></td>
<td>2200</td>
<td>18</td>
<td>16.62</td>
</tr>
</tbody>
</table>
6. CONCLUSIONS

In this work, we presented the algorithm for energy minimization of the hardware codec through E-R-D optimization. The process was implemented in two steps. The first step was the process of E-R-D modeling for the hardware codec which has limited power scalability. To model E-R-D relationships, we selected GOP size and QP as power scalable parameters. From verifying power scalable parameters, power consumption measurement of the hardware codec including SRAM was implemented in gate-level simulation with switching activity. Within the framework, we formulated relationships among energy, rate and distortion by GOP size and QP including external DRAM. In the second step, we proposed the energy saving algorithm for mobile video devices. For the algorithm, we developed a new approach to the system energy model for the hardware encoder including transmission and storage modules. Our experimental results showed that the proposed algorithm saves up to 31.76% of energy consumption while meeting the rate and distortion constraints.

ACKNOWLEDGEMENTS

This work was supported by the Center for Integrated Smart Sensors funded by the Ministry of Science, ICT & Future Planning as Global Frontier Project" (CISS-2013073718)

REFERENCES


